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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/080,568	02/25/2002	Stephen M. Gates	YOR919980324 US2	9141

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/080,568	GATES ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on th cover sh t with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-18,26-31 and 33-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-18,26-31 and 33-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The cancellation of claims 1-10, 19-25 and 32 in Paper filed 5/12/04 is acknowledged.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 11-12, 15-16, 18, 26, 28-29, 33-35 and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durlam et al (US. 5,940,319).

With respect to claims 11-12, 18, 26, 28-29, 33, 35 and 38, Durlam's first embodiment

(Figs. 5-8) discloses an array of microelectronic elements comprising: a substrate of semiconductor material 11; a lower layer of dielectric material (12a,21,25) disposed with a lower surface in contact with the substrate and an upper surface in spaced adjacency thereto; a pattern of mutually electrically isolated conducting regions (19a,37) and (19b,38) (Fig. 5) disposed within the lower layer of dielectric material, the conducting regions extending to the upper surface of the lower layer, an upper layer of dielectric material 51 disposed with a lower surface thereof in contact with and bonded to the upper surface of the lower layer; and a plurality of nodes (43,45) and (44,46) comprising MTJs 43 and 44 and disposed within the upper layer of dielectric material, each of the

nodes being in electrical contact with only one of the conducting regions at the upper surface of the lower layer, wherein each conducting region comprises: a metal conductor 19a and a via 37 formed on the metal conductor 19a and comprising a diffusion barrier material of Ta (not illustrated, see column 3, lines 35-42). It is noted that because the via 37 comprising the diffusion barrier material and because the via 37 extending between the metal conductor 19a and a node (43,45) in the plurality of nodes, the diffusion barrier material would also extend between the metal conductor 19a and the node (43,45) and electrically connecting the metal conductor 19a with the node (43,45).

Durlam's first embodiment does not disclose the plurality of nodes including semiconductor diodes.

However, Durlam further teaches a second embodiment of MRAM (Fig. 17) having a plurality of nodes, which include diodes 93 and 95 in contact with the conducting regions 82 at the upper surface of the lower layer. Accordingly, it would have been obvious to modify the first embodiment by forming the plurality of nodes with the structure as suggested by the second embodiment for the purpose of switching a magnetic memory element to read information in the magnetic memory element (column 6, lines 26-30).

With respect to claims 15-16, Durlam (Fig. 8) further discloses that the device comprises a field effect transistor 12a, a first insulating layer 54 is disposed over an upper surface of the upper layer, and a second insulating layer 33 is formed over the upper surface of the lower layer.

Regarding claim 32, it would have been obvious to form the semiconductor node of Durlam as a field effect transistor because it is an intended use depending upon the application, which is desired for the semiconductor node of Durlam.

Regarding claim 34, Durlam (Fig. 8) also discloses that each of the conductive region further comprises a metal layer 31 (or 24) in electrical contact with the via, the metal layer 31 (or 24) being formed of nickel-iron (column 3, lines 28-30) which is different than the aluminum/copper material of the via 37.

Regarding claims 36-37, Durlam's Fig. 7 further discloses a bonding promoting layer 33 of dielectric material formed on the lower layer 25 of dielectric material, the bonding promoting layer 33 bonding the lower surface of the upper layer 51 of dielectric material to the upper surface of the lower layer 33. As taught by Durlam, the bonding promoting layer 33 is placed between the lower layer 25 and the upper layer 51 to provide electrical isolation between the conductor layers (column 3, lines 60-64). Therefore, it would have been obvious to form the dielectric layer 33 as a glass layer because the glass layer would also provide the electrical isolation between the conductor layers. It is noted that the process limitation (softening temperature in a range of 400 degrees C to 500 degrees c) would not carry patentable weight in a claim drawn to structure because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

3. Claims 13-14, 17, 27 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durlam et al in view of Bronner et al (US. 6,242,770).

Durlam does not disclose that diodes are single crystal Si diodes.

However, it would have been obvious to form Durlam's diodes as single crystal Si diodes because according to Bronner, such single crystal Si diodes (column 9, lines 63-65) would provide high conductivity, high rectification and low total resistance (column 3, lines 1-4).

4. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Durlam et al (US. 5,940,319) in view of Scheuerlein (US. 6,097,625).

Durlam does not disclose the via is filled with the refractory diffusion barrier material.

However, Scheverlein (Fig. 6) teaches the forming of a microelectronic element array comprising an MTJ cell 25 in contact with a conductive region, the conductive region 29 having a metal conductor and a conductive via made of various materials, such as metal or refractory barrier metal alloy of TiSi (column 5, lines 1-8). Accordingly, it would have been obvious to form the via of Durlam with a metal of copper, aluminum or a refractory barrier metal of TiSi because as taught by Scheuerlein, such metal materials would have equivalent in functions of providing the current required to read the cell passes through the conductive region (column 5, lines 1-8).

5. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Durlam et al in view of Baek et al (US. 5,843,837).

Durlam does not disclose the via is filled with the refractory diffusion barrier material.

However, Baek (Fig. 1C) teaches the forming of a conductive via 23 made of various materials, such as metals of Al, Cu or refractory diffusion barrier metals of Ti, Ta

and Mo (column 2, lines 52-54). Accordingly, it would have been obvious to fill the via of Durlam with a metal of aluminum and copper, or with a refractory diffusion barrier metal of Ti, W, and Ta, because as taught by Baek, such metal materials are well known metal materials which are used for the wirings in a conductive contact structure.

Response to Arguments

6. The previous presented claims 11-18, 26-31 and 33-38 do not distinguish over the applied prior art because as discussed in the Advisory Action, mailed on 5/14/04, the applied prior art issued to Durlam does suggest the diffusion barrier material extending between the metal conductor 19a and a node 45 in the plurality of nodes and electrically connecting the metal conductor 19a with the node 45.

In response to Applicant's argument to new claim 39, the new references are applied in the new ground of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
June 25, 2004

PHAT X. CAO
PRIMARY EXAMINER